

APPLICATIONS OF THE CA3228E SPEED CONTROL SYSTEM

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The CA3228E Speed Control System is a monolithic integrated circuit originally designed for automotive cruise control systems; its block diagram is shown in Figure 1. The completeness and self-contained nature of the circuit can be appreciated by examination of the typical automotive application shown in Figure 2. Both I²L logic and linear circuit design are combined to provide the primary functions, feature enhancements and safety backup necessary for a high-performance cruise control system. But its fully facilitated feedback system makes the CA3228E useful in a wider range of applications. The information provided in this Note will aid the user in applying the circuit to applications such as electric motor speed controls, engine speed

controls, and rate controls for manufacturing systems. In fact, any powered system may be controlled with the CA3228E's accelerate or coast to a set speed adjustment and resume speed after braking (or safety stop) adjustment. Special features of the CA3228E include a single command line control and controlled PLL acceleration.

Overview

As shown in the detailed block diagram of the CA3228E in Figure 1, the primary function of the circuit interface to the logic control section is to provide a complement of capability in both linear and logic design. The command decode circuit

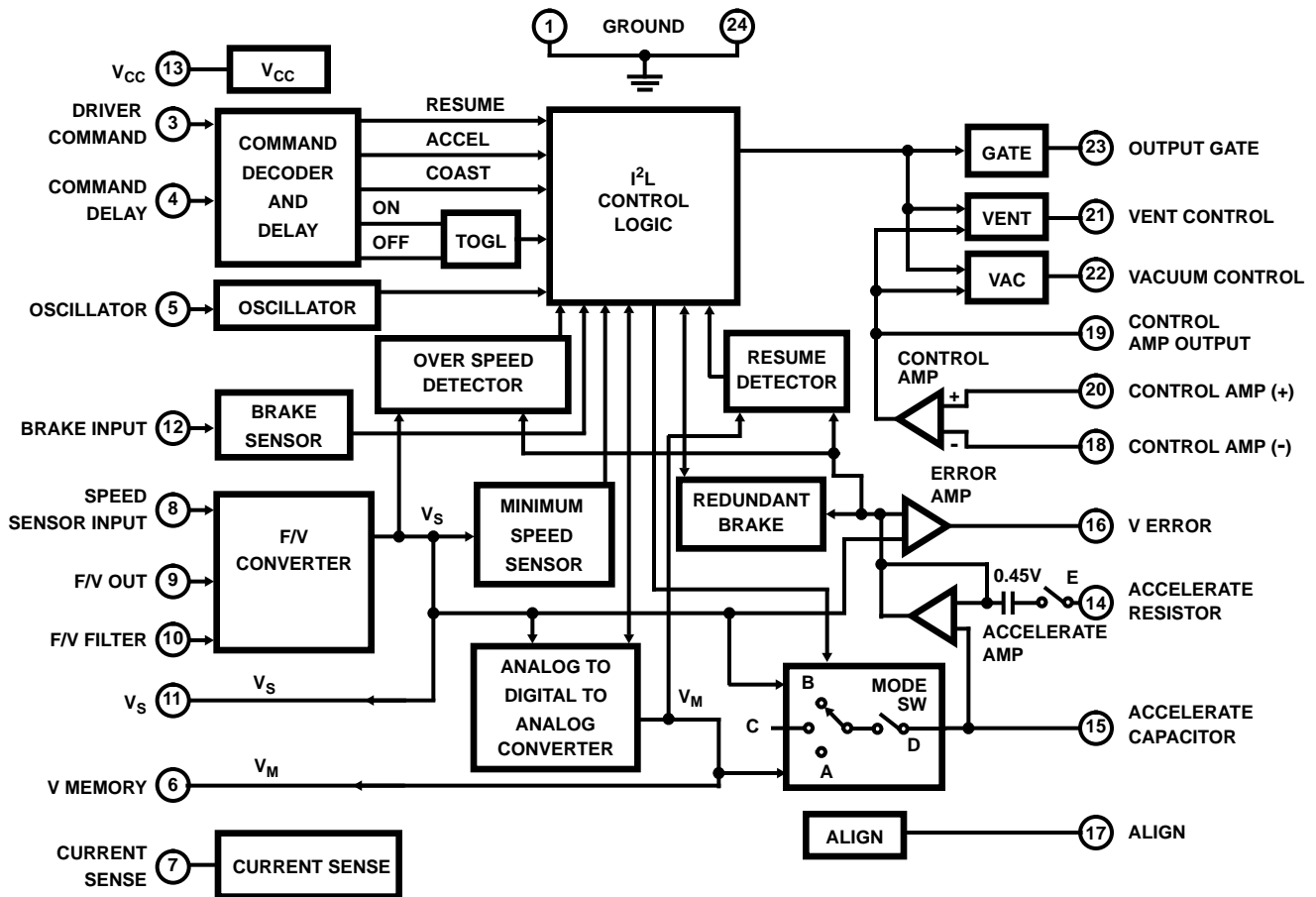


FIGURE 1. BLOCK DIAGRAM OF THE CA3228E SPEED CONTROL SYSTEM

Command and Control Functions

The speed control functions and their descriptions are listed in the following table.

CONTROL	FUNCTION
OFF (Note 1)	Deactivates the device logic and erases memory. $V_3 \leq 0.094 V_{CC}$
ON (Note 1)	Activates device logic and initiates a standby mode, $V_3 \geq 1.1 V_{CC}$ or $+100\mu A$ followed by $V_3 = 0.95 V_{CC}$ (open switches).
SET/ACCEL	Momentary switch closure sets the current speed in memory. Acceleration continues at a constant rate when the switch is held closed. $V_3 = 0.54 V_{CC}$. V_S must be greater than 1.5 V, the minimum speed lockout (MSLT), discussed below, which is approximately 25mph in the system of Figure 2.
COAST	Momentary switch closure sets the current speed in memory. When the switch is held closed, the servo disengages, causing the vehicle to slow-down. When the switch is released, the new speed is stored. During switch contact, $V_3 = 0.21 V_{CC}$.
RESUME (Note 1)	Resumes a cruise condition if the speed is greater than MSLT, a speed has been stored after an on command, and the brake or redundant brake have not been activated. If the speed is greater than the stored memory speed, the coast function will continue until $V_S = V_M$. $V_3 = 0.76 V_{CC}$.
Other control functions that directly affect the operating mode of command setting are:	
BRAKE	At approximately $0.55 V_{CC}$ or more, the brake input, V_{12} , will place the system in standby, but a stored memory speed will be retained. A resume command will return the vehicle to cruise and the previous speed condition.
CLUTCH DISABLE	Same input as brake (for manual transmission).
MSLT (Minimum Speed Lockout)	Minimum Speed Lockout is a low-speed inhibit. This is an internal function that samples the F/V converter output V_S . For V_S approximately equal to $0.183 V_{CC}$ or less, the set/accel, coast, and resume commands cannot be set. In the typical automotive application of Figure 2, MSLT is 25mph.
REDUNDANT BRAKE	If the error amplifier output voltage V_{16} drops below $0.42 V_{CC}$, an internal comparator causes the system to go into the standby mode. This action assures that an excessive error in the servo loop will not cause an unsafe condition by providing an error speed dropout. In the application of Figure 2, the error speed is approximately 11mph.
COMMAND DELAY	To provide immunity to noise and short duration pulses, the set/accel, coast, and on and off switch input hold times are delay controlled to 50ms by a 0.68mF capacitor at pin 4. For each command, a current charge delay is used to counteract switch bounce and to enhance noise immunity. A delay of 330ms is used for the resume command.

NOTE:

1. This control function requires a momentary switch closure.

In addition to the braking and command delay safety features, a gate enable output is available at pin 23. The output at this pin remains low during normal operation of the accel, coast and cruise modes; however, it goes high for the brake, redundant brake, and low speed lockout (MSLT) commands, and during the high speed dropout condition of the resume mode. The normal applied circuit use of this feature is shown in Figure 2, where a low on the gate output at pin 23 permits the vent and vacuum drivers for the solenoid actuators to conduct through a saturated transistor common to the emitter of each driver. Should either the vacuum or vent driver transistor fail, the gate transistor would act as a safety backup, since it would be cut off and thereby mandate a standby condition.

Command Decoder Input Circuit

The command decoder input circuit is shown in Figure 3. Driver commands and their ranges of control are shown in Figure 4. Initially, the logic must be activated to an on and active standby state. This is done by setting the input emitter of Q38 at pin 3 to a higher voltage level than the V_{CC} supply line in the IC. The current should be safely limited by using a $10k\Omega$ resistor in series with pin 3. A current of $100\mu A$ is more than sufficient to cause Q38 to conduct current to Q37, the transistor switch that activates the on state condition. A bias divider at pin 3 (shown in Figure 2) of 560Ω and $10k\Omega$ establishes the command idle position after each momentary switch closure is completed.

When switch contact is made and the pin 3 bias levels are properly set, four comparators select the resume, accel, coast and off driver commands. An internal resistive divider is used to bias one input of each comparator, while the other input is biased from pin 3. As shown for the off comparator, in which I_{20} and I_{21} interface to the I^2L logic, each of the comparators drives the I^2L logic through switching transistor gates. The logic section of the IC determines all further control requirements from the state of the four comparators.

The control switching time is affected by the command delay circuit associated with pin 4 (Figure 1) and the charging time of the $0.68\mu F$ capacitor at pin 4. The $0.68\mu F$ capacitor sets command delays of 50ms, except for the resume command which is $330\mu s$. The delay time is determined from two states of constant current drive to pin 3. Longer or shorter times may be set by changing the value of the pin 4 capacitor, but the ratio of other command delays to resume will remain the same. To calculate the capacitor value needed to change the time delay to the one desired, use the following equation:

$$V = It/C \text{ or } C = It/V$$

where V is voltage, I is current, C is capacitance, and t is time. Since V and I remain fixed, equation matching yields:

$$C1/C2 = t1/t2$$

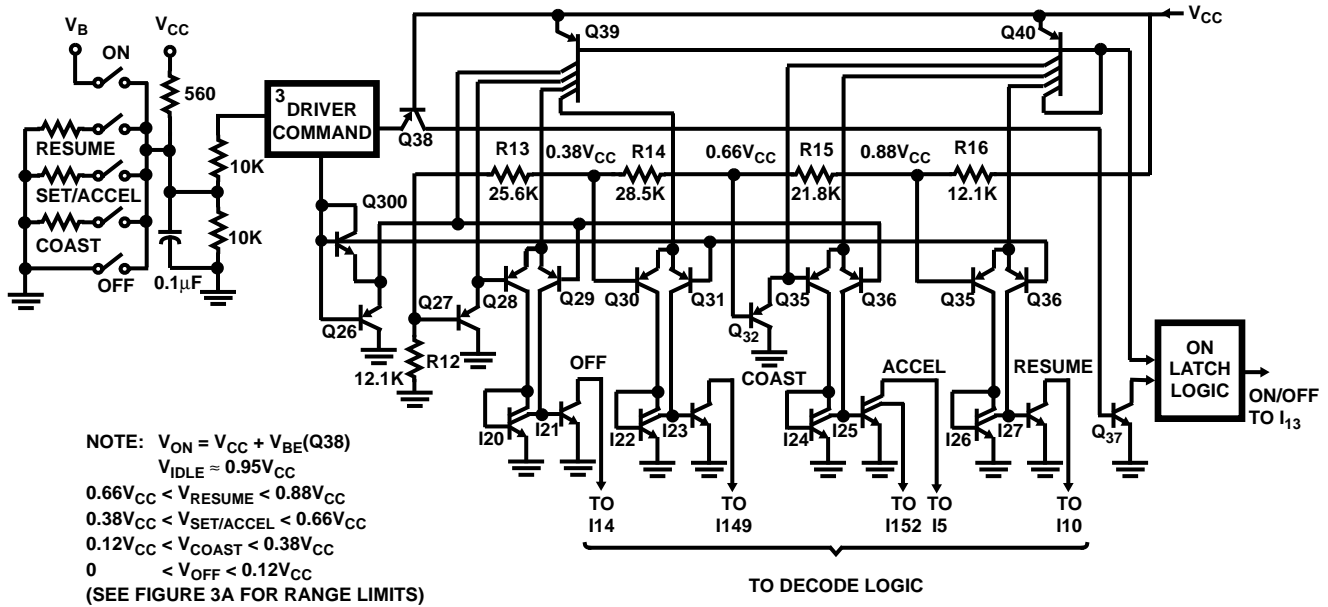


FIGURE 3. DRIVER COMMAND INPUT COMPARATOR CIRCUIT AND LOGIC OUTPUT TO COMMAND DECODE

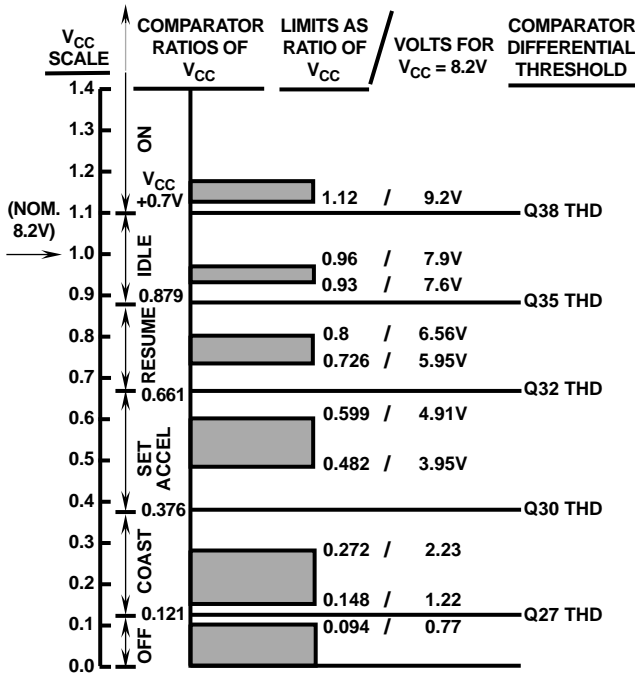


FIGURE 4. DRIVER COMMANDS AND THEIR RANGES OF CONTROL

Frequency-to-Voltage (F/V) Converter Operation

The schematic of Figure 5 shows the circuit of the F/V converter portion of the CA3228E. The input at pin 8 is

normally the speed input from a speed sensor of the moving system. In normal use of the operating system, a frequency is applied at pin 8, which is a scale multiplier of the controlled system speed. For the circuit of Figure 2, the scale is 2.22Hz/mph and, with the components shown biasing the F/V converter, the conversion gain from pin 8 to pin 10 is typically 27mV/Hz. Under these conditions, the system performance parameters of the data sheet apply, including a normal speed-control range of 62 to 222Hz. In calibrating a normal range of F/V control for the V_S (pin 10) output, the frequency range in terms of voltage becomes 1.67 to 6V. Typical voltage range values of 1.5V minimum to 6.8V maximum are possible at the V_S output.

Figure 6 demonstrates the flexibility and range of design capability of the converter function by showing converter range possibilities for various values of C8 and C9; the capacitors are selected to accommodate a given range of input frequencies. The capacitor at pin 8 is chosen primarily as a filter to provide good noise immunity. Resistor R₈ and capacitor C8 provide both DC and AC overvoltage protection. The normal range of sensor input voltage is 3.5 V_{PP} minimum to 15 V_{PP} maximum.

As indicated by the capacitance versus frequency plot of Figure 6, the range of input frequencies may be changed; however, the minimum to maximum frequency ratio will always remain approximately the same. As an example, assume that it is desired to center the range of input frequencies at approximately 1000Hz. At this frequency, C9 should be approximately 0.005μF and C8 approximately 0.01μF. For these values, the minimum frequency at a V_S of 1.5V is 500Hz; the maximum frequency at a V_S of 6.8V is 2400Hz.

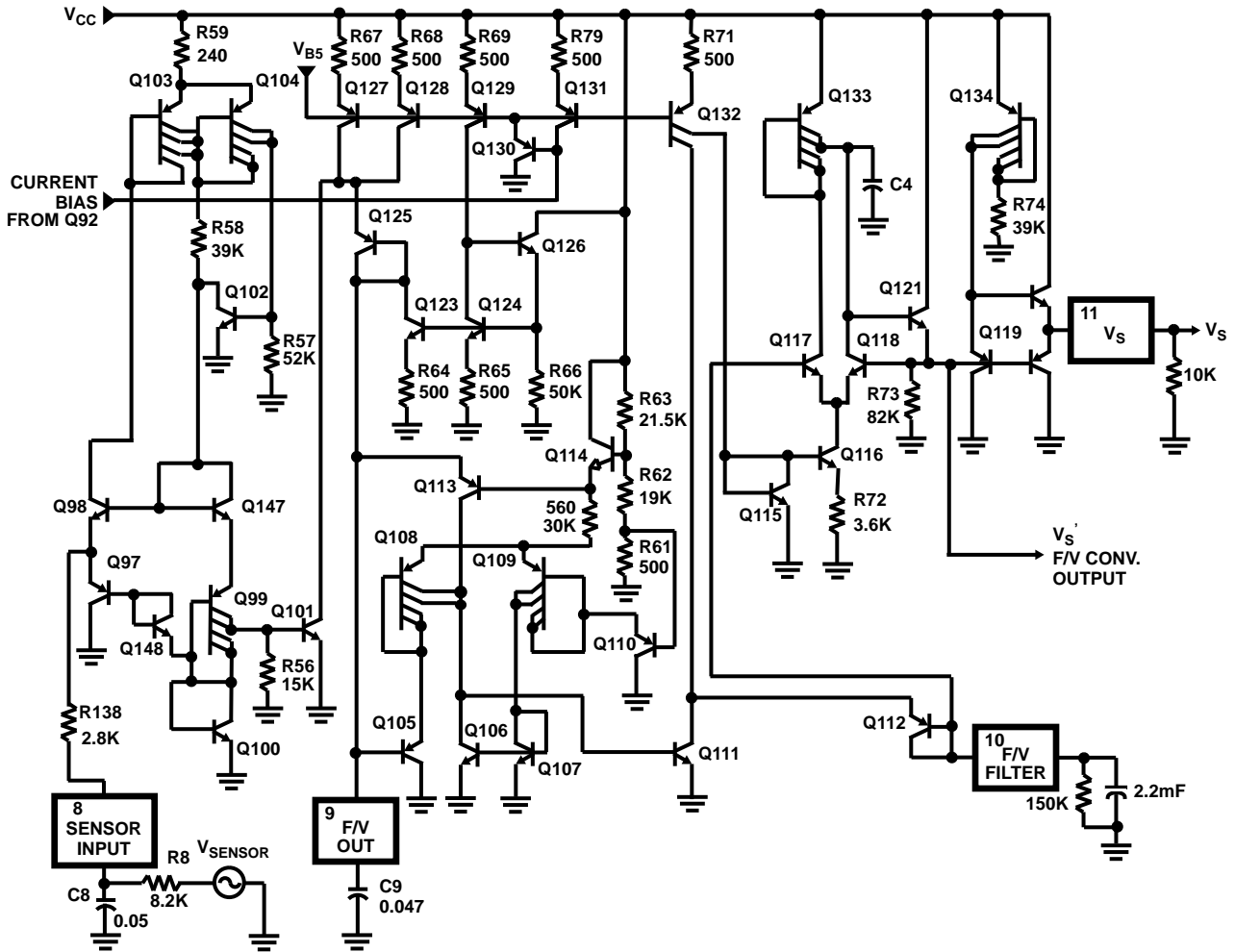


FIGURE 5. FREQUENCY TO VOLTAGE (F/V) CONVERTER CIRCUIT

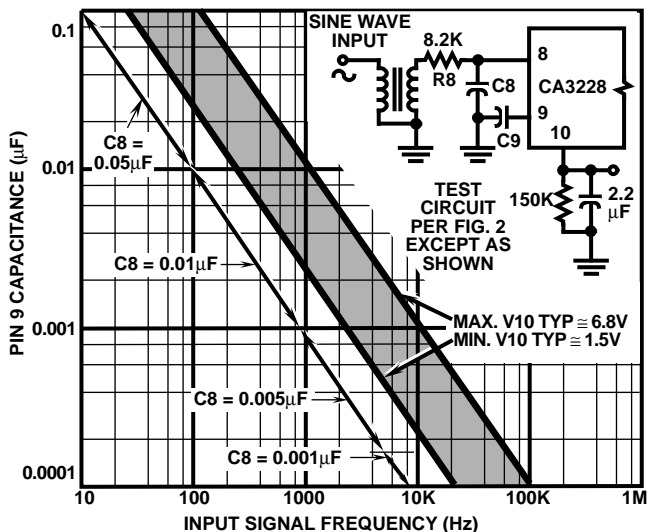


FIGURE 6. F/V CONVERTER RANGE EXTENSION WITH ADJUSTMENT OF C8 AND C9

It is possible to extend the frequency range of the F/V converter to frequencies as low as 10Hz and as high as 500kHz. However, the loop stability of the lower frequencies may be difficult to control. Higher values become very dependent on

stray capacitance, causing some loss of output linearity where the internal circuit becomes bandwidth limited.

Input signal requirements at pin 8 are characterized by the voltage versus current characteristic of Figure 7. While the VI curve may appear to be complex, the drive requirement is explained simply by noting that the pin 8 input shown in Figure 5 is made through a 2.8kΩ resistor to the emitters of an n-p-n and a p-n-p transistor. When the signal input voltage polarity goes negative, Q98 conducts and changes the state of a latched current mirror (Q102, Q103, and Q104). The changing mode of the current source reflects back to the base of the input n-p-n transistor Q98, changing the DC level at pin 8. This change of state occurs when pin 8 is slightly negative (approximately $1 V_{BE}$). The abrupt change to a positive voltage of approximately $2 V_{BE}$ is normal.

The requirements of this change of state have some influence on the design of the source input drive to pin 8. For the F/V converter input stage to switch properly, a current source drive such as an inductive pickup device or a transformer coupled signal source is preferred. In any case, it is important to note that the signal should swing negative to fully activate the change of state. It is also preferred that the input signal be nearly centered with respect to the voltage zero

crossing. The external series 8.2kΩ resistor at pin 8 must be used to limit peak currents, particularly when inductive pickup sensors are used. Inductively coupled circuits may produce transient pulses if any intermittent condition exists.

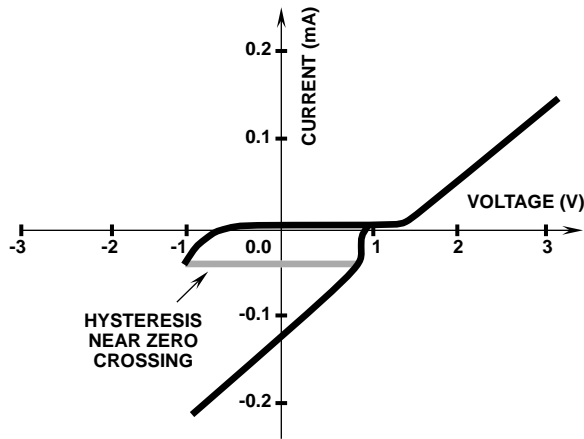


FIGURE 7. F/V CONVERTER INPUT CHARACTERISTIC PIN 8 VOLTAGE vs. CURRENT

As shown in the functional diagram of Figure 8, the second stage of the F/V converter is a pair of current generators that are used to produce both positive and negative ramp slopes when driven by the square-wave signal from the output of the first stage (at the collector of Q101). As shown in Figure 9, the capacitor at pin 9 is charged and discharged by the fixed current sources which develop a truncated ramp signal of approximately 4 V_{PP}. The ramping signal is applied to a window comparator with reference points of 0.482 V_{CC} at the emitter of Q113 and 0.012V_{CC} at the base of Q105 (see Figure 5). When the ramp is in the transition range between these voltage levels, a high output pulse (from an equivalent 2 input NAND gate) drives the base of Q111. The comparator levels are determined from a resistor divider: R61, R62, and R63. The peak signal level is approximately 4V, while the minimum signal swing is nearly at ground level. The pulse width provided at the collector of Q111 is a function of the ramp transition time.

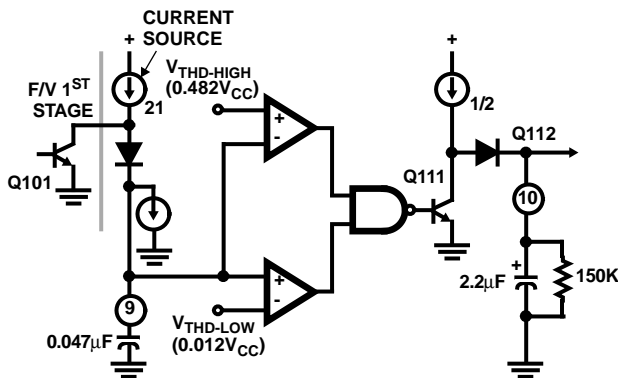


FIGURE 8. F/V CONVERTER COMPARATOR STAGE

Since a pulse of fixed width is generated on each positive and negative transition of the input signal at pin 8, it remains to integrate the pulses to produce a DC voltage proportional to the input frequency. The integration is accomplished in the

RC filter circuit of pin 10. Diode Q112 rectifies the current-driven pulses developed at the collector of Q111.

Another important characteristic of the F/V converter is the absence of pulses from Q111 when no signal is present at pin 8. Diode Q112 remains reversed biased by any positive DC voltage applied to pin 10. Therefore, it is also possible to use a DC voltage signal input at pin 10 to directly control the servo feedback system. In many PLL control systems, a DC voltage signal is easily generated from position indicators. In the CA3228E, this capability provides the user with an alternative to some of the restrictions that apply to the use of the F/V converter, restrictions that may require frequency dividing to accommodate the desired frequency range and bandwidth limitations on the chip.

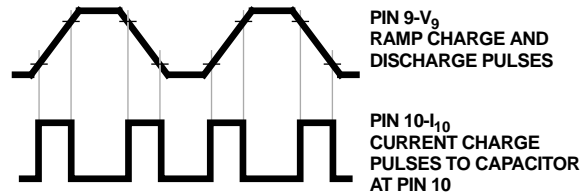


FIGURE 9. PIN 9 F/V OUTPUT AND F/V FILTER SIGNAL AT PIN 10

The range of the applied signal at pin 10 should be approximately 2V to 6V. The input impedance at pin 10 is quite high due to the source follower stage that follows the pin 10 input and drives Pin 11 plus the V_S' output to the A/D converter and mode switch circuits. Pin 11 is a sample test point for the F/V converter output, V_S. The V_S' signal is separately buffered and output to the A/D converter and mode switch circuits.

To provide a stable temperature characteristic for the F/V converter voltage, external control of the current-source generator has been provided. In the CA3228E, pin 7, Figure 10, represents a temperature-stable external sensitivity control point for the F/V converter output voltage V_S. The 43kΩ temperature-stable metal-film resistor used to bias pin 7 drives the F/V converter current sources. The current drive generated in the emitter of Q92 by this resistor provides a mirror-current bias to the F/V converter current-ramp circuits.

A/D Converter and Memory Update Comparator

The signal V_S', derived from the F/V converter output, Figure 5, and the D/A converter signal, V_M, are internally fed to the memory-update comparator circuit of Figure 11. The V_M signal may be monitored at pin 6. As noted in Figure 5, the V_S' signal is also fed to pin 11 through a buffer amplifier. The signal at pin 11 is the F/V converter output, V_S, and has a close tracking relation to V_S', when pin 11 is biased with a 10kΩ resistor to ground. In Figure 11, the V_M and V_S' signals drive buffer amplifiers Q276 and Q277, respectively. From Q274 and Q271 the V_S' signal is sent to the error amplifier, over-speed detector and mode switch. The V_M signal is sent to the mode switch via Q275 and Q269. The V_S' mode switch input (Figure 13) is at Q231 and the V_M input is at Q232. Transistors Q269 and Q271 also drive Q268 and Q270, the memory update comparator input transistors.

The block diagram of Figure 12 provides a broader perspective on the total operation of the D/A converter and stored memory operation by showing the signal flow by function. In Figure 12, the voltage developed by the F/V converter is V_S at the pin 11 monitor output, and is labeled as V_S , at the internal input to the memory update comparator. When, at a chosen speed, the accel/set or coast switch is depressed and then released, the command logic clears the register and initiates clocking in the ripple counter. Clocking continues and successively increases the D/A converter current output in increasing stair step increments until the V_M voltage resulting from the product of the current and the R38 resistor value is equal to V_S .

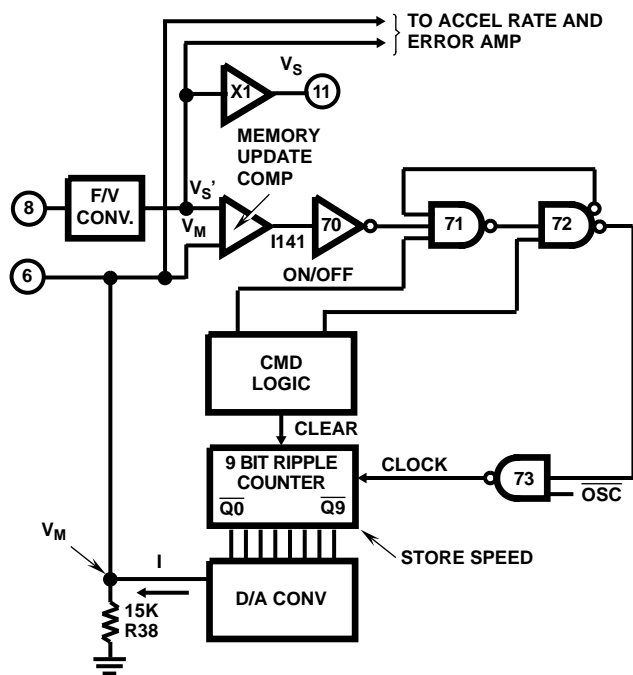


FIGURE 12. MEMORY UPDATE COMPARATOR WITH MEMORY AND D/A CIRCUITS

When $V_M = V_S$, the memory update comparator changes state and sends a signal through output I141 to the logic circuit to stop the clocking of the 9-bit ripple counter. The stored bits in the ripple counter continue to bias the D/A converter to produce the memory set V_M speed reference. Any further changes in V_S , are compared to the V_M output of the D/A converter, which then provides the error signal for the servo control. (Refer to the Command and Control Functions section of this Note, above, for complete details of the command inputs that affect the stored speed setting.)

The circuit of Figure 10 shows a portion of the 9-bit ripple counter and the D/A circuit driven by the counter. Each cell of the 9-bit counter has a Q_x output that drives its respective current source. When the counter is active, the summed outputs of the D/A converter driven current generators are present on the V_M line and at pin 6.

Mode Switch and Acceleration Control

The mode switch of Figure 13 is that portion of the CA3228E whose inputs for V_S' and V_M are Q231 and Q232, and whose output is through pin 15. Logic commands control the mode switch by controlling Q248, switch A; Q237, switch B; and Q250, switch D. When switch A is activated, Q248 is off, which allows Q232, Q240, Q241, and Q245 to conduct the V_M signal to pin 15 and the base of Q251. Similarly, V_S' is conducted to pin 15 via Q231, Q233, Q234 and Q244 when switch B (Q237 off) is activated.

In the accel mode, switch D is open, allowing the acceleration-rate amplifier to dictate a controlled rate of acceleration. A switch D open corresponds to an active high signal from I100, which causes Q250 to conduct, and which, in turn, causes Q243 to conduct. The Q243 output to Q242 is then at an emitter-base saturation level and Q242 is cut off, which prevents Q244 and Q245 from conducting V_S' , or V_M to pin 15 and Q251.

Switch D is also open during resume ramp conditions. Note that V_S' and V_M are in tracking modes when Q250 is open and Q242 is conducting. The V_M tracking mode is the closed-loop cruise mode. The V_S' tracking mode applies to conditions other than cruise, accelerate, and resume. In the V_S' or V_M tracking modes, Q235 or Q246 supplies current to the base of Q242. The Q242 collector output supplies the current that charges the capacitor at pin 15.

The acceleration-rate amplifier controls a fixed rate of acceleration by providing an internal charging voltage and an external RC time constant at pins 14 and 15. When the acceleration circuit is active, Q135 is off and current source Q261 conducts current through Q266. Current-mirror circuits also control current through R132 and produce a fixed voltage offset in the signal path from pin 14 through Q266, R132, and Q263. In the active accelerate mode, an offset voltage is present at the bases of Q251 (pin 15) and Q257. The offset signal that is present at the base of Q257 is also the output of the acceleration rate unity gain source follower amplifier. The voltage generated across resistor R132 is approximately 0.45V, and is the charging voltage for the external resistor and capacitor. The typical values of the external R and C are 2.4MΩ and 2.2μF. Since the acceleration voltage that charges the external circuit is constant, linear approximations to the rate of change may be used. Using the equation:

$$V = It/C$$

$$V/t = I/C \cong 0.45/RC$$

Since V in the equations represents a fixed velocity-error voltage, $V/t = 0.45/RC$ represents a fixed rate of acceleration. It is therefore possible to change the acceleration rate by adjusting the RC values. The desired rate of acceleration is based on system factors associated with the servo feedback loop. The values shown in this Note are for a typical automotive application. Since very low currents are used, the capacitor must also have a low leakage. For the conditions shown in Figure 2, charging current is 0.188μA.

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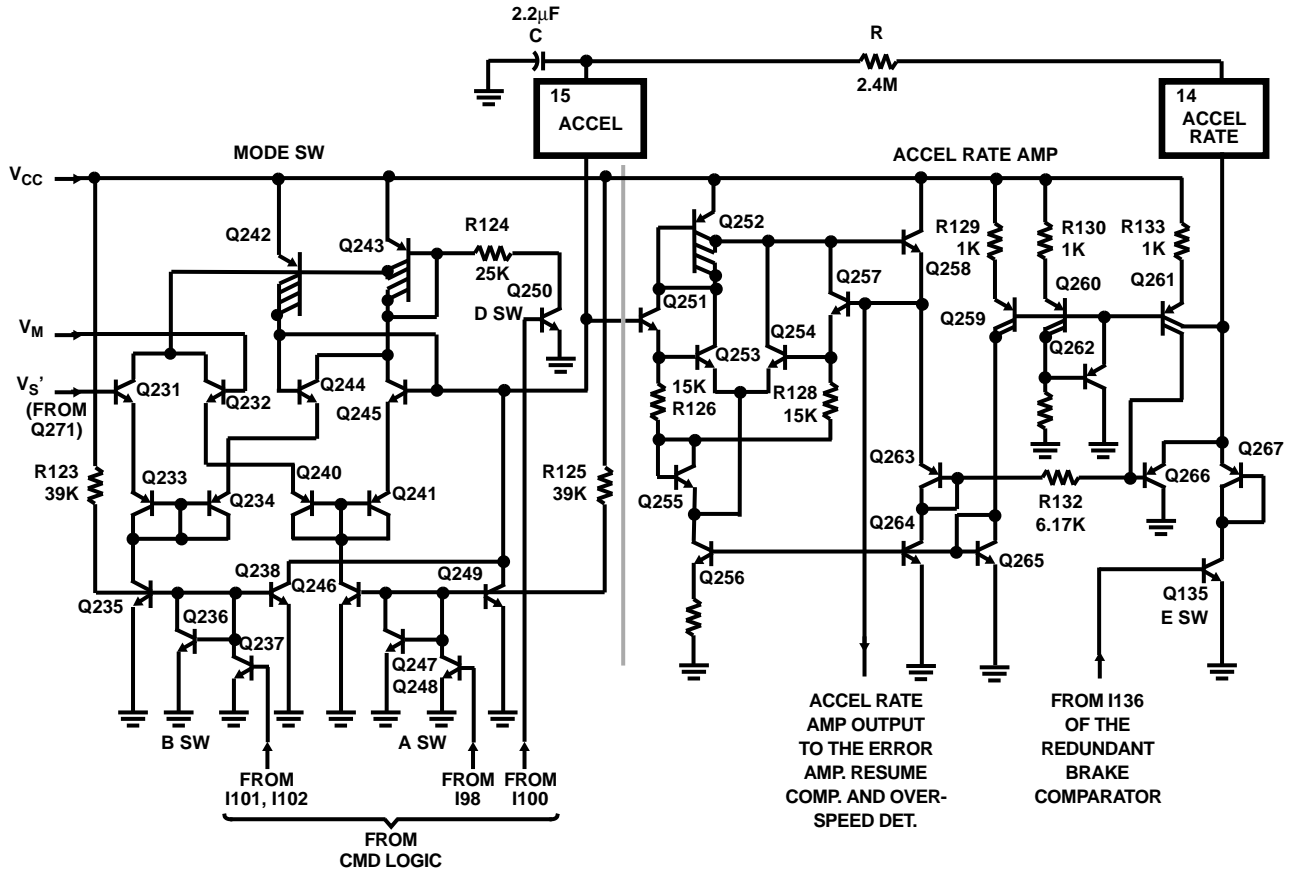


FIGURE 13. MODE SWITCH AND ACCELERATION-RATE AMPLIFIER CIRCUIT

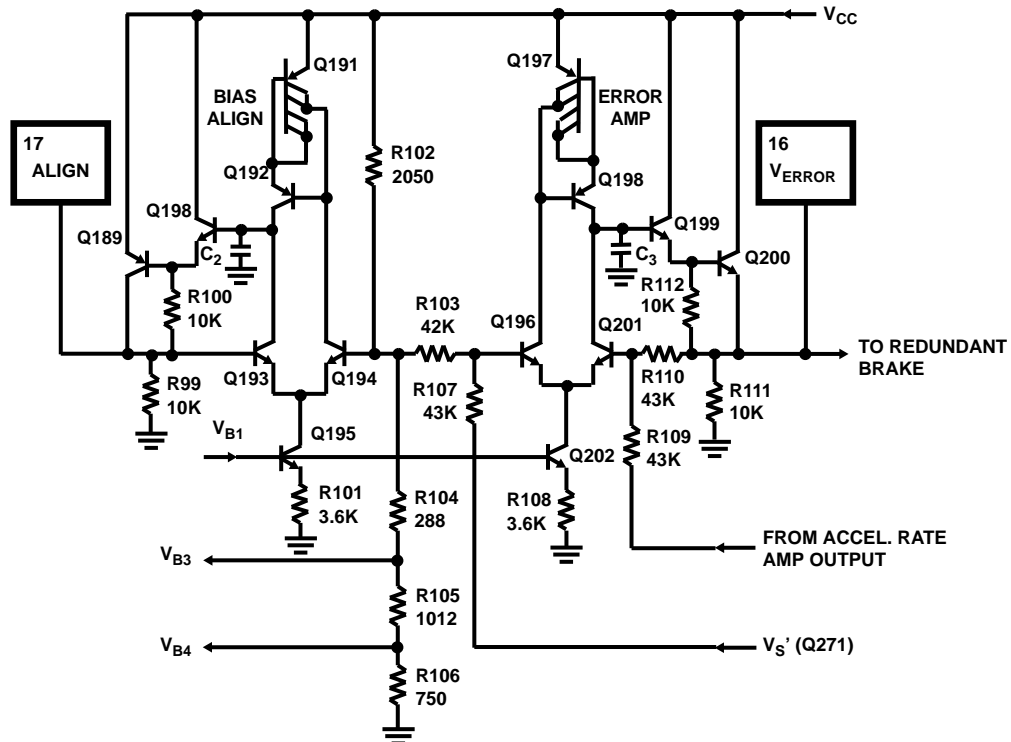


FIGURE 14. ERROR AMPLIFIER SHOWN WITH BIAS "ALIGN" SETUP CIRCUIT

Error Amplifier

The output signal of the acceleration rate amplifier is fed to the error amplifier, the overspeed detector, and the resume comparator. Under normal cruise conditions, the error amplifier continues to correct speed errors when V_S' deviates from V_M .

The error amplifier, Figure 14, is a part of the signal flow path of the feedback loop. The amplifier has an internal differential input and an output at pin 16. When the system is in a V_S' tracking mode, V_S' is present at both inputs. When the system is in a V_M tracking mode, the error signal is present at pin 16. The output signal of the error amplifier is externally coupled to the control amplifier at pin 18. Internally, the error amplifier output is fed to the redundant brake comparator. The error amplifier serves the error summing function of the servo loop and, as such, is a unity gain source follower.

The bias "align" function circuit is shown with the error amplifier circuit in Figure 14. The output at pin 17 is $0.5 V_{CC}$ and may be used for bias and setup. Current drain at pin 17 should not exceed 1mA.

Control Amplifier

The control amplifier shown in Figure 15 receives the signal from the error amplifier output at pin 16. Pin 18 is the negative input with respect to the control-amplifier output at pin

19, and pin 20 is the positive input with respect to the same output. The control amplifier may be regarded as a normal op amp whose gain is controlled with external feedback. However, the output signal is also internally coupled to the output vent, vacuum, and gate driver circuits. The open-loop gain, A_{OL} , of the control amplifier is typically 800. Figure 16 shows the control-amplifier bias configuration with pin 20 connected to an external divider at approximately $0.5V_{CC}$ and a variable feedback to pin 18. In the normal input circuit for pin 18, as noted in Figure 2, R16 and R19 are typically $10k\Omega$ and $1M\Omega$, respectively.

Because the vent and vacuum driver amplifiers have a gain dependent controlled deadband, the feedback versus gain characteristic of the control amplifier is as shown in the curve of Figure 16. The curve follows the classic feedback gain equation and is approximately equal to $R19/R16$ for ratios less than 50. However, the approximation is less accurate for ratios in the 100 range where the error is 15%. The feedback versus gain characteristic of the application circuit of Figure 2 is typically centered at a ratio of 100. Figure 17 shows the deadband of the output vent and vacuum amplifiers as a function of the $R19/R16$ ratio; the output drive circuits are discussed in further detail in the following.

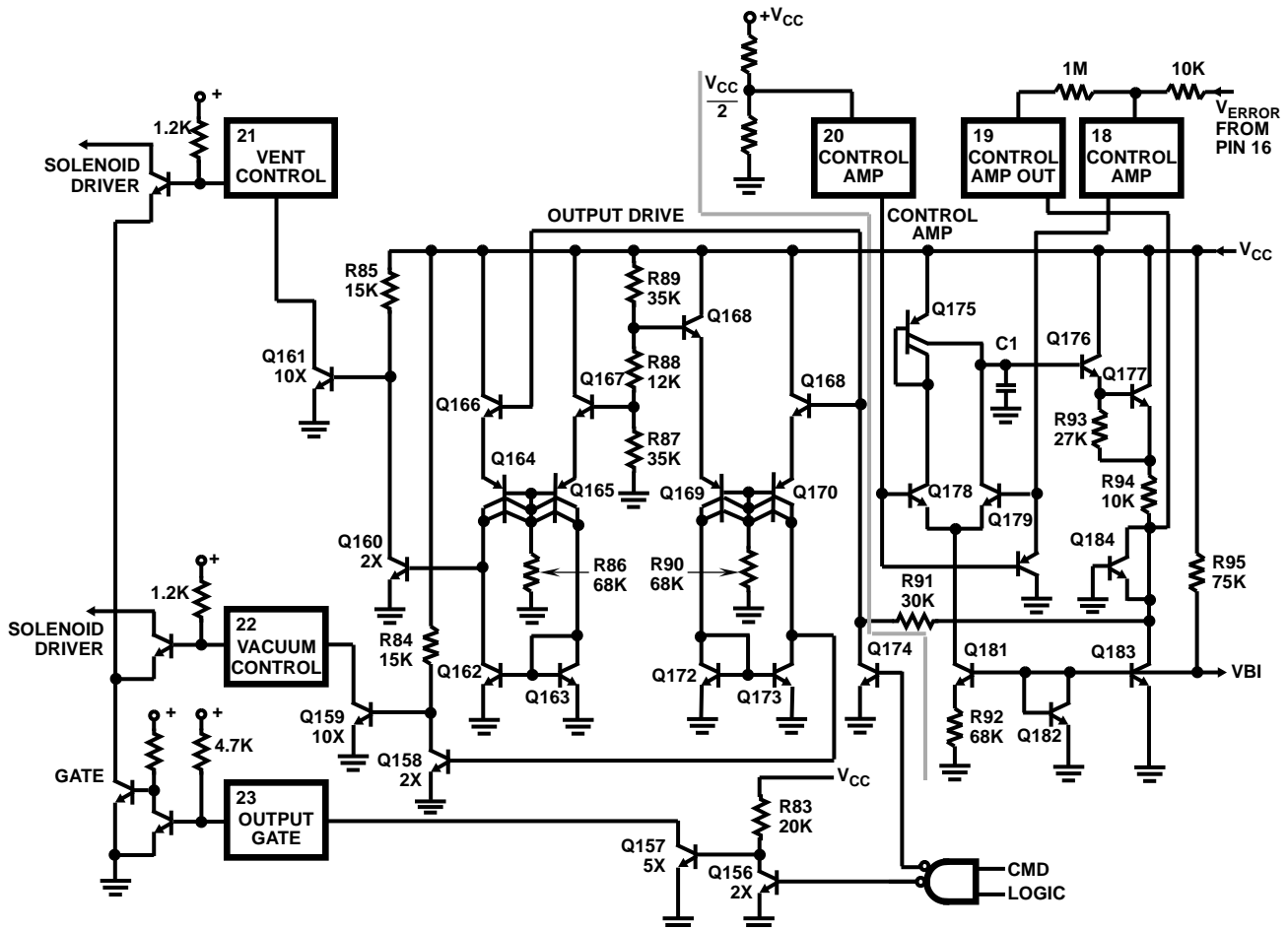


FIGURE 15. CONTROL AMPLIFIER AND OUTPUT DRIVERS

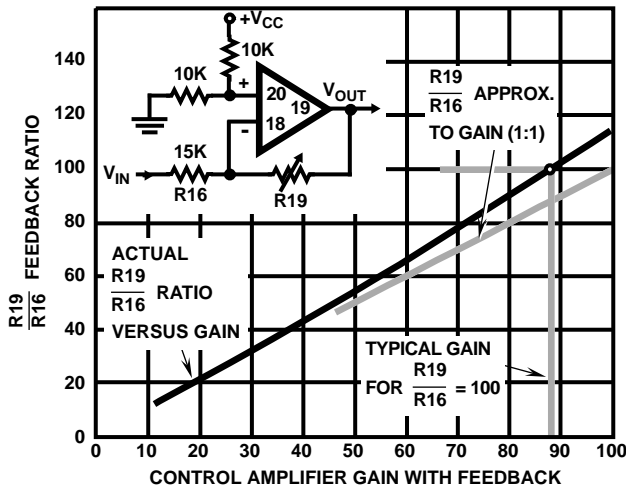


FIGURE 16. CA3228E FEEDBACK RATIO VERSUS CONTROL AMPLIFIER GAIN (WITH FEEDBACK)

Output Drive Circuits

The nomenclature of the output-drive circuits has been chosen to represent a normal vacuum-controlled actuator. Vacuum control of the actuator is intended to provide acceleration while vent control provides a relaxation or coast function. The output-drive circuits consist of amplifier drivers for the vent, vac (vacuum), and gate-output terminals at pins 21, 22, and 23, respectively, as shown in Figure 15.

A single input from the control amplifier controls the vacuum and vent outputs. The signal is passed through R91, a 30kΩ resistor, and the base of Q171 to a differential amplifier that controls the vacuum output. The base of Q171 is also common to the base of Q166, which is the differential-amplifier input that controls the vent output. The differential amplifiers for the vacuum and vent functions have reference inputs tied to a resistor divider composed of R87, R88, and R89.

The tap ratio for the Q168 input (comparator reference for the vacuum output) is at 57%. The tap ratio for the Q167 input (comparator reference for the vent output) is at 43%. When the control amplifier input is less than 0.43 V_{CC}, both vacuum and vent drivers are switched low or remain in a saturated on state. They remain on as long as the divider tap voltages are higher than the control amplifier input voltage. This situation defines a relaxed servo or coast mode.

When the control amplifier input voltage exceeds the 0.43 V_{CC} tap level, the Q166 differential input voltage forces the base of Q160 and the collector of Q161 at the vent output to switch high. While the vent output is high and the vacuum output low, the system is in the deadband, which is the normal cruise mode. However, as the control-amplifier input voltage is further increased to the 0.57 V_{CC} tap level, both the vent and the vacuum outputs are switched high. The vacuum output switches to the high state when the base input of Q171 exceeds the 57% tap reference for Q168 and causes Q159 to switch off. When both the vent and vacuum outputs are high, the system is in a state of acceleration. As noted on Figure 2, the state of each mode is dependent on the external normally open (N.C.) and normally closed (N.C.) solenoid polarities.

The above action assumes that the gate output is low, permitting the external drive circuits of Figure 2 to function normally. The gate output remains low for acceleration, cruise, and coast functions. For brake, redundant brake, overspeed and minimum speed conditions, the gate output is high, which prevents acceleration and forces the system into a noncontrollable state. The gate output is forced high, and the vacuum and vent outputs low, by an internal logic switch, I103, that disables the output drivers.

The deadband of the output drive circuit is fixed by resistor ratio, but can be controlled through the gain of the control amplifier. It should be noted that measurement of the deadband or tap ratio points requires forcing of the drive voltage to the control amplifier and measuring of the voltage at pin 19 when the vacuum and vent outputs change state. The circuit of Figure 2 was used to generate the curve in Figure 17, which shows the variation of the deadband range when the gain of the control amplifier is changed by changing external feedback. The deadband range is shown in Figure 17 in a mV spread as a V_S reading at pin 11. As the control amplifier gain is made to approach unity, the deadband approaches the actual tap voltage separation of 1.19V when V_{CC} equals 8.2V.

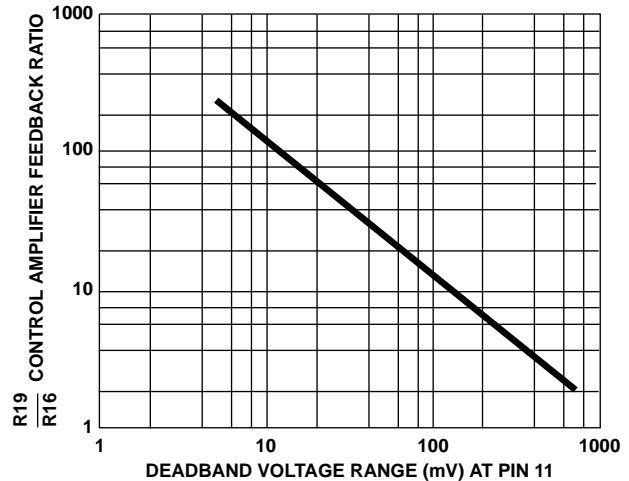


FIGURE 17. DEADBAND VOLTAGE RANGE IN OUTPUT CIRCUIT AS A FUNCTION OF CONTROL AMPLIFIER FEEDBACK RATIO (GAIN ADJUSTMENT) REFERENCED TO V_S AT PIN 11

Redundant Brake

When the speed-control system is in the cruise mode, the redundant brake comparator (shown in Figure 18) may become active if significant error voltage develops at the output of the error amplifier. Specifically, if loading or braking is causing the speed of the system to be reduced, the redundant brake comparator senses that the speed is falling off. When the error developed reaches a difference speed of 11mph, the redundant brake comparator switches logic gate I136, which causes the system to go to the standby mode. More generally, when the voltage at pin 16 drops below 42% of the V_{CC} supply voltage, I136 switches state. There is an additional output from the redundant brake through I135; this output remains high during cruise and acceleration modes. I136 inhibits the acceleration rate amplifier by controlling the E switch. (Also see Figure 11.)

The conditions that determine the operation of the brake and redundant brake can be determined from the acceleration and sensitivity factors discussed above. The sensitivity of the F/V converter is approximately 27mV/Hz. For the system of Figure 2, the system magnetic speed sensor ratio is 2.22Hz/mph. Multiplication of these factors yields a ratio of 59.94mV/mph. Dividing this ratio into the 450mV offset designed into the acceleration rate amplifier provides a result of 7.5mph. Comparison of this result to the 11mph error allowed before the redundant brake becomes effective indicates that there is a wide enough safety margin to prevent redundant braking during acceleration.

A special feature of the CA3228E prevents extraneous noise from switching the redundant brake output and causing the system to go into standby. This feature is provided by a 4-bit shift register that is used as a digital filter to clock all four outputs of the shift register to 1's before a 4-input AND gate can switch the logic to standby.

Brake Input Comparator

The brake input comparator, also shown in Figure 18, is a comparator amplifier driving an inverter logic gate (I142). When the brake input is greater than $0.55 V_{CC}$, as determined by the resistor divider composed of R77 of 20kΩ and R75 of 24.5kΩ, the I142 gate output changes state. The brake input is normally connected through a current limiting resistor to the brake switch, and is in parallel with the brake light. The change of state at the output of the brake input comparator drives the command decoder which places the system in standby.

Minimum Speed Lockout

The minimum speed lockout (MSLT) comparator shown in Figure 11 senses the speed voltage V_S' , and compares it to the output of a fixed resistor divider. When V_S' drops to less than 1.5V, the comparator switches, which sends a signal to the control logic that places the system in standby. If V_S' is initially less than 1.5V, the system cannot be set in the cruise mode. The divider ratio of $0.183V_{CC}$ is approximately 1.5 V for a normal V_{CC} of 8.2V. For a speed sensitivity factor of 59.94mV/mph, 1.5V is equivalent to 25mph.

Overspeed Detector and Resume Comparator

The associated functions of over speed detector and resume comparator are shown in Figure 19. From the normal condition, where a speed is set in memory and cruise is being maintained, it may be desired to increase speed and then return to the cruise mode. If the range of speed increase is large, it is best not to use the accel mode but to manually accelerate to the higher speed and then press the set/accel switch. An over speed detector comparator compares V_S' and V_M and controls the logic to assure a smooth transition.

During acceleration, V_S' is greater than V_M . When the set/accel command is given, the logic turns on Q250 (Figure 13) and the capacitor at pin 15 is rapidly charged. When the voltage at pin 15 is within 60mV of V_S' , the over speed detector output is switched low. At that point, further V_S' correction is assumed by the acceleration-rate amplifier under fixed-rate conditions. The overspeed detector maintains the 60mV off-

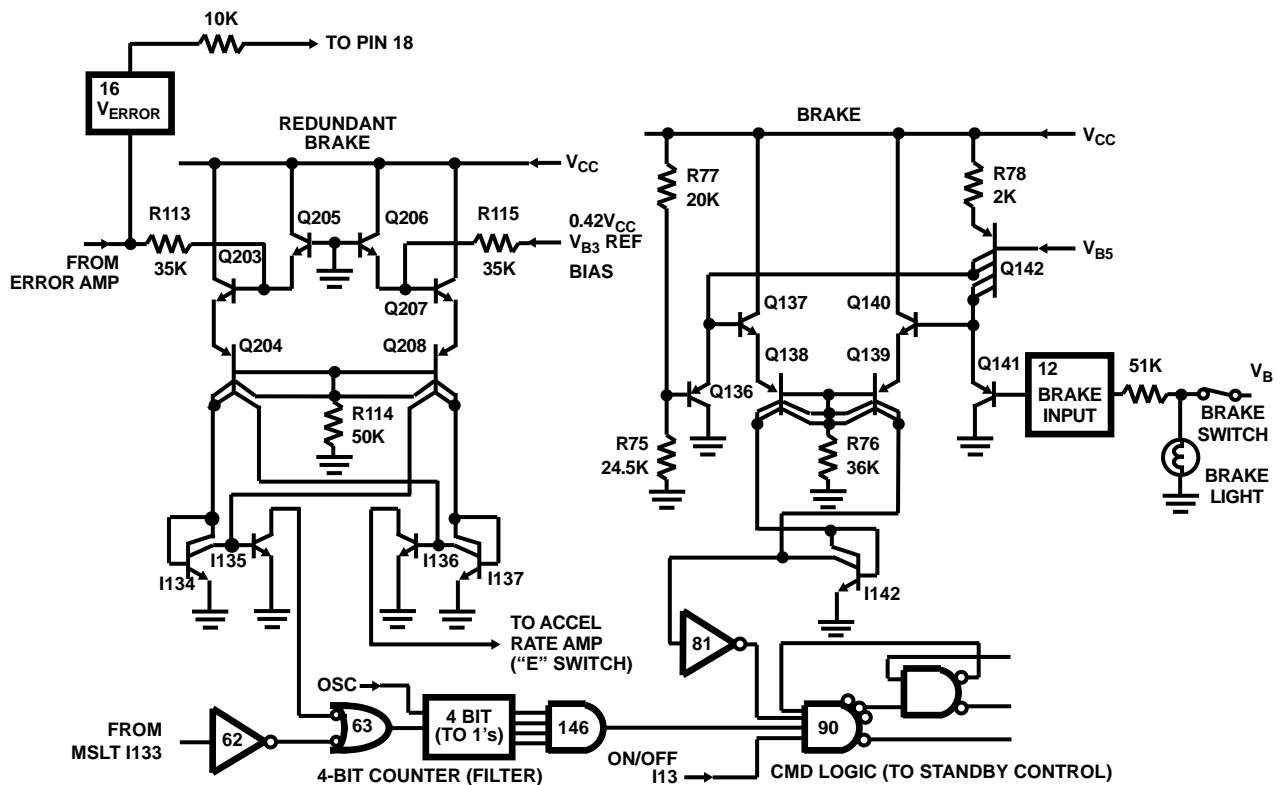


FIGURE 18. BRAKE AND REDUNDANT BRAKE

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set along with a sufficient amount of hysteresis to assure noise immunity. When cruise conditions have been disrupted by braking action, and it is desired to return to cruise, the driver presses the switch for resume. The resume comparator samples V_S' and V_M and determines the fixed acceleration required for return to the speed previously stored in memory. An internal filter is used at the output of the comparator to prevent noise from resetting the comparator before V_S' reaches V_M .

Oscillator (Clock) Circuit

The circuit of Figure 20 shows the RC oscillator circuit used for internal clocking of the 9-bit ripple counter and the 4-bit counter that serves as a digital filter for the redundant brake. Various other elements of the command logic require oscillator control for the toggling of flip-flops. The oscillator frequency is an independent internal function on the chip, and has no relation to the frequency of the F/V converter input. A single capacitor at pin 5 determines the oscillator frequency. However, the fixed current source noted as V_{B5} also has an effect. The V_{B5} current source is derived from the same bias line that controls the F/V converter current sense drive from a 43k Ω resistor at pin 7. While the oscillator frequency may be changed by adjusting the resistor at pin 7, this adjustment will also change the F/V converter sensitivity. Since the volt-

age bias at pin 7 is approximately 5.5V, Q130 and Q131 are driven by 128 μ A through Q92 in the F/V converter (see Figure 5). The base bias line for Q131 is V_{B5} , and is mirror connected to Q84 and Q85 in the oscillator. A charge current of 128 μ A goes to the 0.001 μ F capacitor at pin 5 from p-n-p transistor Q85. A 4x current mirror n-p-n transistor, Q86, discharges current at 512 μ A from the capacitor at pin 5. The resistor divider at the base of Q81 switches between 4.1V and 6.1V as I144 and Q85 are toggled on and off in the return feedback loop. With a charge current of 128 μ A and a discharge current of 512 μ A and using the equation:

$$t = VC/I$$

the clocking time, t , (and hence oscillator frequency) can be calculated using the 2V change for V , a 0.001 μ F capacitor value for C , and the charge and discharge currents for I . The result is 15.6 plus 3.9 μ s or a frequency of approximately 51kHz.

Operation and Performance

Table 1 defines the voltage values for the pins of the CA3228E IC. The annotations cover pins where conditions may be expected to vary. For further detail on the functions of the V_M and V_S' voltages at pins 6 and 11, respectively, refer to the CA3228E data sheet.

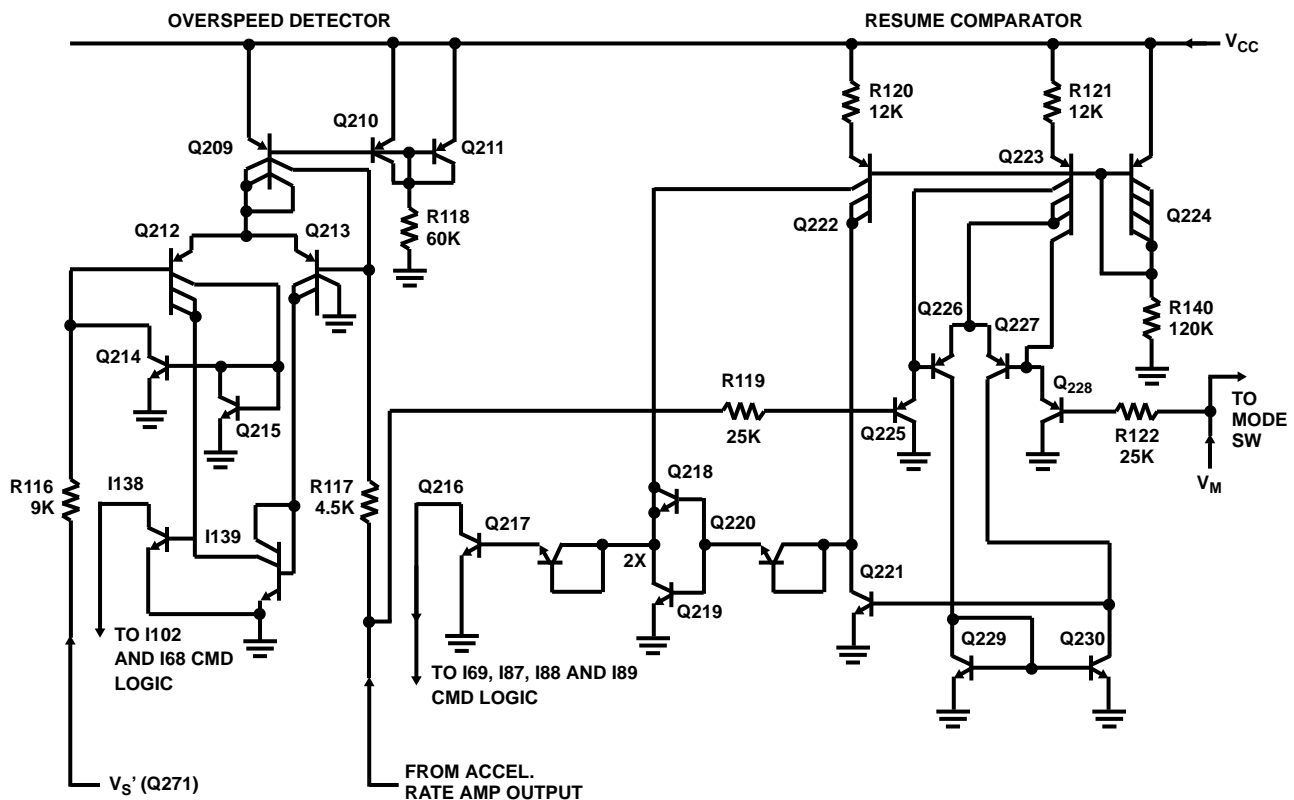


FIGURE 19. OVERSPEED DETECTOR AND RESUME COMPARATOR

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TABLE 1. NORMAL CRUISE-MODE PIN VOLTAGES FOR THE CA3228E (NOTE 1)

PIN NO.	VOLTAGE	PIN NO.	VOLTAGE
1	Ground	13	8.2V Normal V_{CC} Supply Voltage
2	No Connection	14	4.55V
3	7.76V (Idle)	15	4.1V, 0.45 Less Than V_{15} in Accelerate Mode
4	0.01V	16	4.1V
5	$5.2 V_{DC}$, V_{AC} Sawtooth 4.1 to 6.1V	17	4.1V
6	1.5 to 6.5V, Speed Dependent (0V without Memory Set)	18	4.1V
7	5.45V	19	4.1V (Product of Error Voltage and Gain)
8	$\cong 0V_{DC}$, $\cong 2.5V_{AC}$	20	4.1V
9	4V Peak AC Signal	21	8.2V, Active Low
10	0V to 6.5V, sSpeed Dependent, Equal to V_6 in Cruise Mode	22	0.06V, Active High
11	Same as V_{10}	23	0.025V
12	0.01V with Brake Switch Open	24	Ground

NOTE:

- $V_{CC} = 8.2V$, speed set at 60mph ($V_6 = 3.6V$).

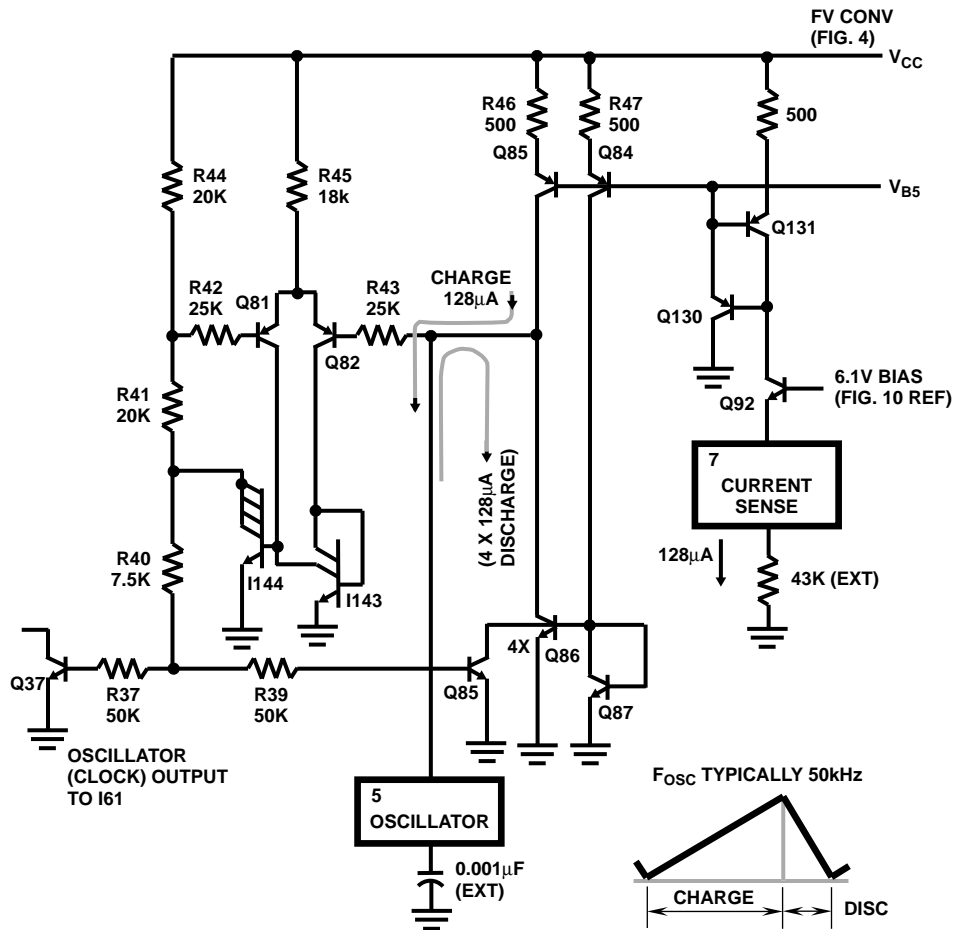


FIGURE 20. OSCILLATOR CIRCUIT USED FOR INTERNAL D/A CLOCK DRIVE

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Note that the D/A converter cannot be set at low speeds and will remain at or near 0V until the frequency at pin 8 is near 50Hz (for the conditions of Figure 2). Dynamic signals are present at pins 5, 8, and 9. Speed dependent voltages are present at pins 6, 10, and 11. Error dependent signals have a notable effect on control amplifier output at pin 6 and the driver output pins 21 and 22. The command input at pin 3, the brake input at pin 12, and the gate output at pin 23 are mode dependent. The table does not reflect all of these changes since the conditions are noted only for a normal cruise setup at approximately 60mph. Again, the data sheet has further details on the various mode and state changes.

It is important to remember that the mode inputs are momentary touch switches except for the hold down condition of the accel and the coast switches. If pin 4 is monitored during the command input changes, it will be noted that delay switching times noted in the data sheet will be reflected at this pin.

Measures of the operating performance of the CA3228E are the wide power supply and temperature-operating ranges. The curve of Figure 21 shows the dynamic range of the power supply input V_{CC} at pin 13 over the temperature range of -40°C to $+120^{\circ}\text{C}$. The normal V_{CC} specified is $+8.2\text{V} \pm 0.8\text{V}$ or approximately 10% tolerance. The curves of Figure 21 also demonstrate a wide tolerance in the minimum to maximum range over which the device functions. A failure, as noted in the figure, is defined as a phase-locked-loop malfunction. Note that even with the wide range shown for power supply tolerance, it is still recommended that an external zener regulator or equivalent be used at the V_{CC} power supply input. Vehicular power supply conditions typically range from 9V to 16V, a range that exceeds the maximum range and rating for the operation of the CA3228E. While some applications may work at lower voltages than the recommended 7.4V minimum, operating conditions should not exceed the 9V power supply maximum rating.

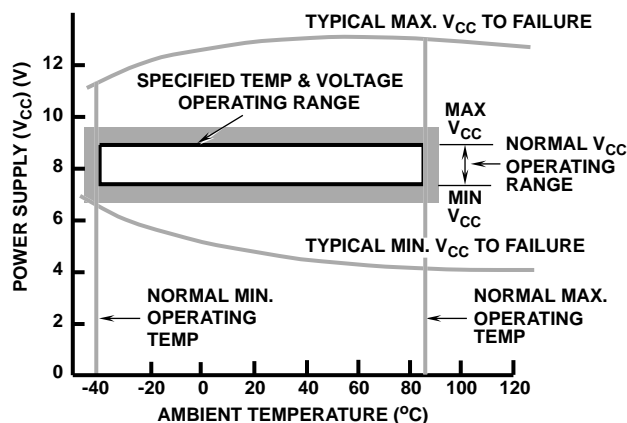


FIGURE 21. V_{CC} OPERATING RANGE OF THE CA3228E

Figure 22 shows another wide-range capability of the CA3228E when the temperature is varied. The V_S and V_M voltages are plotted versus temperature from -60°C to $+100^{\circ}\text{C}$. Both the voltages for V_S and V_M are shown along with the equivalent speed condition for the typical application of Figure 2. For the 59.94mV/mph quoted above, the

voltages of 4.3 to 4.5 are 72 to 75mph, respectively. It should be noted that Figure 22 is a measured curve from -55°C to $+90^{\circ}\text{C}$ with an equivalent 73.5 ± 1.5 mph error. Over the same range, the V_S and V_M readings typically tracked within 130mV while maintaining a cruise mode.

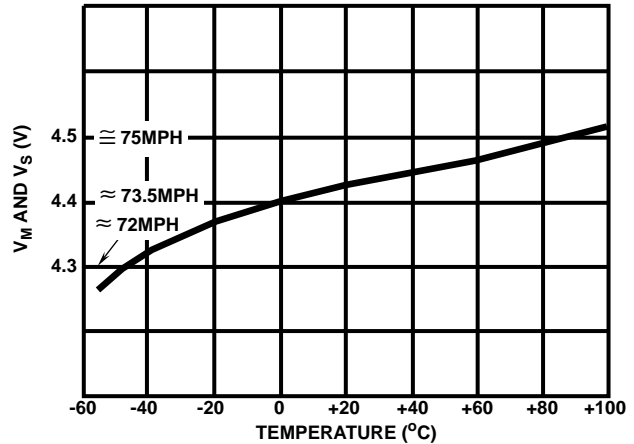


FIGURE 22. TYPICAL CHARACTERISTIC OF THE F/V CONVERTER OUTPUT, V_S , AND D/A OUTPUT, V_M , TRACKING vs TEMPERATURE IN THE CIRCUIT OF FIGURE 2

General Applications

A CD4046 CMOS VCO (voltage controlled oscillator) may be used in the external loop to drive the sensor input at pin 8. In the closed-loop circuit shown in Figure 23, the CA3228E will respond to the accelerate, cruise and coast conditions and provide the appropriate drive at the vacuum and vent outputs. From an idle mode after turn-on, the frequency may be adjusted by the 1M Ω potentiometer. The adjustable range of the potentiometer output to the VCO input at pin 9 is ground on the low end to V_{CC} on the high end. The 0.047 μF capacitor between pins 6 and 7 and the 100k Ω resistor at pin 1 were chosen to accommodate a frequency range of 50 to 250Hz.

When a VCO frequency representing a given speed is set by the frequency control and applied to the sensor input at pin 8, the set value may be entered into the CA3228E D/A memory with the set/accel command. Changing the switch at pin 9 of the CD4046 to the loop position then closes the servo loop with the VCO set frequency retained in the D/A memory. The PLL of the CA3228E will maintain the frequency of the VCO, and any conditions that force the VCO off frequency will be corrected by cruise or resume mode control.

While the VCO closed-loop circuit was used to demonstrate the capability of the CA3228E, it is also apparent that many applications of the referenced circuit or variations of this circuit may exist.

Sketches of various application possibilities for the speed control system are shown in the functional diagrams of Figure 24. These applications have not been reduced to practice but are only suggested possible circuits. Since the MSLT and redundant brake affect the low end settings, a diode bias clamp of

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1.6V should be used at pin 11 to keep V_S higher than the minimum speed lockout level. Pseudo DC voltage levels can be applied to pin 10 to set a V_S level for the D/A memory.

Further potential for use of the speed control system includes its combination with the CDP68HC05 series micro-processor control systems with added memory and D/A control.

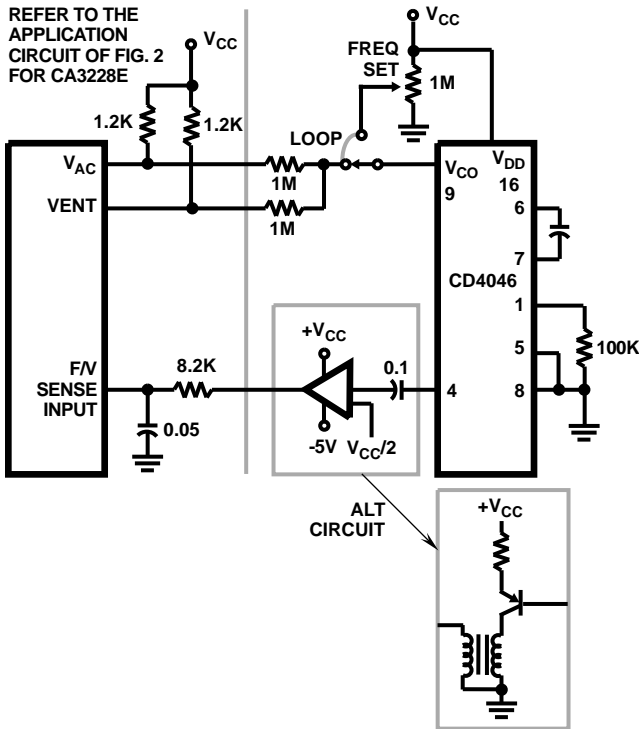


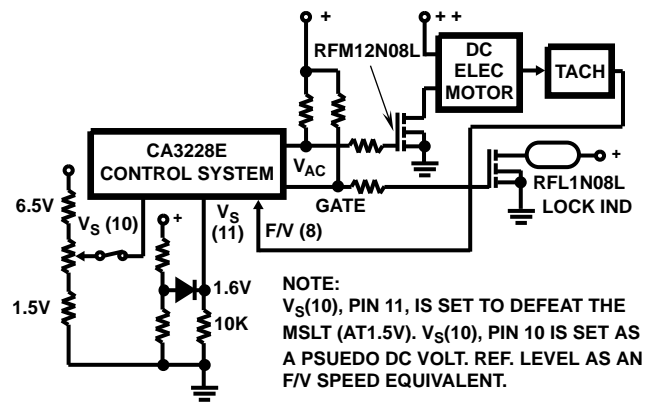
FIGURE 23. PLL OSCILLATOR FREQUENCY CONTROL CIRCUIT

References and Bibliography:

1. "CA3228E Speed Control System," Harris Data Sheet, File No. 1436.
2. "New Chips That Simplify Motor Control," L.J. Hadley, Machine Design, Feb. 12, 1981.
3. "A Monolithic Speed-Control Micro-System For Automotive Applications," R.B. Jarret and W.D. Pace, ISSCC, 1978.

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NOTE:
 $V_S(10)$, PIN 11, IS SET TO DEFEAT THE MSLT (AT 1.5V). $V_S(10)$, PIN 10 IS SET AS A PSEUDO DC VOLT. REF. LEVEL AS AN F/V SPEED EQUIVALENT.

FIGURE 24A.

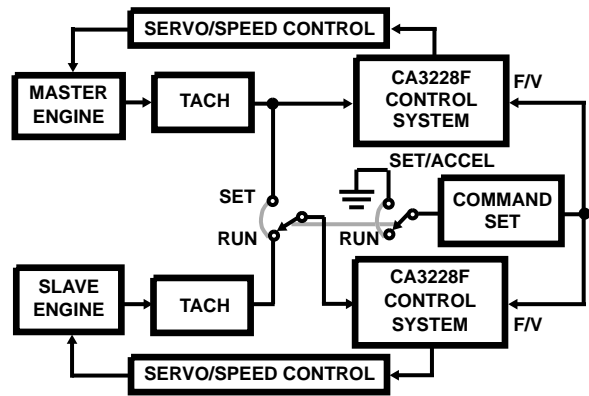


FIGURE 24B.

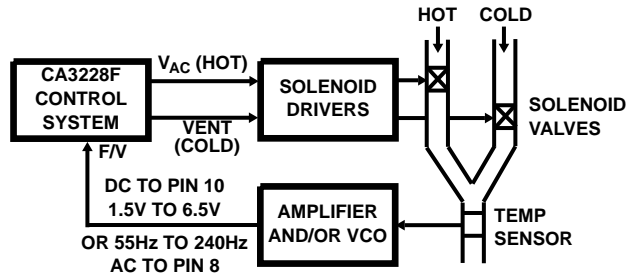


FIGURE 24C.

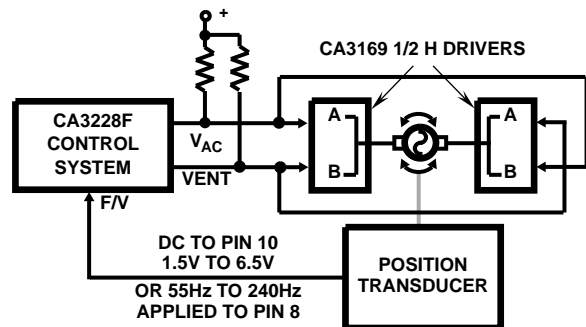


FIGURE 24D.

FIGURE 24. SUGGESTED APPLICATIONS OF THE CA3228E: A. DC MOTOR SPEED CONTROL, B. MASTER/SLAVE ENGINE SPEED CONTROL. SWITCH TO SET/ACCEL TO STORE MASTER SPEED IN SLAVE D/A MEMORY, THEN SWITCH TO "RUN". C. AIR OR FLUID TEMPERATURE CONTROL. (SEE A. FOR V_S SETUP CIRCUIT.) D. DC MOTOR POSITION CONTROLLER. (SEE A. FOR V_S SETUP CIRCUIT.)